In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**
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REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application.

The independent claims have been amended as helpfully suggested by the Examiner to overcome the current prior art references. In addition, the independent claims have been amended to correct the grammatical error as helpfully noted by the Examiner. New dependent Claims 53 and 54 are being added; these claims correspond to previously cancelled Claims 29 and 30.

The claim amendments and remarks supporting patentability of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 20, for example, is directed to a method of transmitting data between a master device and a slave device via a clock line and at least one data line, with the clock line being maintained by default on a first logic value. Each master and slave device is able to tie the clock line to a potential representing a second logic value opposite the first logic value. The method comprises:

when the master device is sending data to the slave device and the slave device is receiving the data from the master device, then

the master device applies data to the data

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line, then ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data,

the slave device maintains the tie to the clock line at the second logic value while the slave device has not read the data,

the slave releases the tie to the clock line at the second logic value when the slave device has read the data, and

the master device maintains the data on the data line at least until an instant when the clock line is released by the slave device,

the master device releases the data on the data line after the clock line is released by the slave device and by the master device; and

when the slave device is sending data to the master device and the master device is receiving the data from the slave device, then

the master device ties the clock line to the second logic value,

the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and then or simultaneously applies the data to the data line,

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the master device maintains the tie to the clock line at the second logic value while the master device has not read the data,

the master device releases ~~release~~ the tie to the clock line at the second logic value when the master device has read the data,

the slave device maintains the data on the data line at least until an instant when the clock line is released by the master device, and

the slave device releases the data on the data line after the clock line is released by the master device and the slave device,

with the slave device tying the clock line to the second logic value every time the master device has tied the clock line to the second logic value, regardless of the direction in which the data is transmitted.

The present invention may advantageously provide a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself. The slave device advantageously ties the clock line to the second logic value

every time the master device has tied the clock to the second logic value.

Independent Claim 48 is directed to a synchronous data transmission system, and has been amended similar to independent Claim 20.

II. The Claims Are Patentable

The Examiner rejected independent Claims 20 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification.

The Examiner has taken the position that FIG. 4-2 on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (SCK=0 at SCK Edge No. 1). The Examiner also characterized the SPI Block Guide as disclosing that the clock line is tied to the second logic value, via the two devices, after data is applied to the data line (data is applied before SCK Edge No. 1), and data on the data line is maintained by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (data is applied until rising edge of clock).

As correctly noted by the Examiner, the SPI Block Guide fails to disclose that the tie to the clock line is maintained by the device to which the data is sent while the

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device has not read the data. The Examiner cited the SMBus Specification as disclosing this feature. In particular, the Examiner referenced FIG. 4-7 on page 22 in section 4.3.3.

In view of the amended claims, the Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. The SMBus Specification discloses that the slave device ties to the clock line only when it is not ready to handle data transfer.

In sharp contrast, the claimed invention recites that the slave device ties the clock line to the second logic value every time the master device has tied the clock line to the second logic value, regardless of the direction in which the data is transmitted. In the Applicants' application, the master device does not apply data bits to the data line while the clock line is not on 1 (i.e., on the second logic value). When the clock wire is on 0, this means that the slave device is not ready to receive the data bits. This means that the sending of new data bits by the master device is subject to the "authorization" of the slave device, and that this authorization is only acquired from the moment the clock line is released (is on 1).

Accordingly, it is submitted that amended independent Claim 20 is patentable over the SPI Block Guide in view of the SMBus Specification. Amended independent Claim 48 is similar to amended independent Claim 20. Therefore, it is submitted that

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this claim is also patentable over the SPI Block Guide in view of the SMBus Specification.

In view of the patentability of amended independent Claims 20 and 48, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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